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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/086,717	03/04/2002	Shigeru Nakamura	H-1034	2183

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EXAMINER	
ZARNEKE, DAVID A	
ART UNIT	**PAPER NUMBER**
2827	

DATE MAILED: 04/30/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/086,717	NAKAMURA ET AL.	
	Examiner	Art Unit	
	David A. Zarneke	2827	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 February 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *8-12,14-17,19 and 20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *8-12,14-17,19 and 20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

In the response filed 2/17/04, Applicant presented two arguments disputing the rejection of pending claims 8-12, 14-17, and 19-20.

Applicant's first argument with respect to claim 8 has been fully considered but is not persuasive. It was argued that Hiroyuki and Takiar fail to teach the pressure electrical connection of the protruding electrodes of the first chip with their corresponding electrodes on the substrate.

The examiner asserts that Takiar does indeed teach the pressure connection of the protruding electrodes of the chip with their corresponding electrodes on the substrate. As discussed in the previous office action, in column 10, lines 34-43, Takiar teaches the pressure connection of the protruding electrodes of the chip with their corresponding electrodes on the substrate.

Applicant's arguments with respect to claims 17 and 20 have been considered but are moot in view of the new ground(s) of rejection. It is argued that Hiroyuki fails to teach the mold as having a ventilation hole on the side opposite the resin injection entrances.

Seeing as this is a newly submitted limitation, the examiner has searched as considered this limitation and has found art with which to reject these claims, as discussed below.

Claim Rejections - 35 USC § 103

The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

Claims 8, 14, 15 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hiroyuki et al., JP 2000188369, in view of Takiar et al., US Patent 5,422,435.

Hiroyuki teaches a device comprising:

(a) preparing a wiring substrate (4) having a plurality of electrodes (6) created on a main surface thereof;

(b) preparing a first semiconductor chip (1a) having a main surface, a back surface, a plurality of semiconductor devices created on said main surface of said first semiconductor chip and a plurality of protruding (10, 34-43) electrodes created on said main surface of said first semiconductor chip;

(c) preparing a second semiconductor chip (1b) having a main surface, a back surface, a plurality of semiconductor devices created on said main surface of said second semiconductor chip and a plurality of electrodes created on said main surface of said second semiconductor chip and having a thickness smaller than a thickness of said first semiconductor;

(d) placing said first semiconductor chip on said main surface of said wiring substrate with said main surface of said first semiconductor chip facing to said main surface of said wiring substrate in such a way that said protruding electrodes provided

on said main surface of said first semiconductor chip face said respective electrodes provided on said main surface of said wiring substrate;

(e) after said step (d), electrically connecting all of the protruding electrodes simultaneously with corresponding electrodes of the wiring substrate while applying a pressure to said back surface of said first semiconductor chip;

(f) after said step (e), placing said second semiconductor chip on said back surface of said first semiconductor chip so as to make said back surface of said second semiconductor chip face said back surface of said first semiconductor chip through an adhesive by applying a pressure smaller than said pressure applied in said step (e);

(g) after said step (f), electrically connecting said electrodes created on said second semiconductor chip to said respective electrodes provided on said wiring substrate by using a plurality of wires, respectively; and

(h) forming a resin sealing body (5) for sealing said first semiconductor chip, said second semiconductor chip and said wires (Figures 4 & 5).

Hiroyuki fails to teach (1) the application of pressure to 1st chip so as to electrically connect it to the electrodes of wiring substrate and (2) the pressure applied to the 2nd chip being smaller than the pressure applied to the 1st chip.

Takiar teaches a stacked multi-chip module (figure 5) comprising providing a carrier member (152), such as a lead frame (5, 26+), or a substrate having leads thereon (8, 25+), on which a 1st chip (146) is pressure adhered, a 2nd chip (148) pressure adhered to the 1st chip using a pressure smaller than the pressure used to apply the 1st chip (10 34+).

It would have been obvious to one of ordinary skill in the art at the time of the invention to use the pressure bonding of Takiar as the method of bonding the chips in the invention of Hiroyuki because pressure bonding is a conventionally known in the art method of bonding chips or substrates.

The use of conventional materials to perform there known functions in a conventional process is obvious. In re Raner 134 USPQ 343 (CCPA 1962).

Regarding claim 14, Hiroyuki teaches applying solder balls (6) to the back side of the wiring substrate (Figures).

With respect to claims 15 and 16, Takiar teaches applying a 3rd chip to the substrate and a 4th chip on top of the 3rd chip (Figure 10).

Claims 9 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hiroyuki et al., JP 2000188369 in view of Takiar et al., US Patent 5,422,435 as applied to claim 8 above, and further in view of Lau, Flip Chip Technologies 1996, McGraw-Hill, p. 302-303.

Hiroyuki and Takiar both fail to teach the use of heat along with pressure to bond chips and or substrates together.

Regarding claim 9, the application of heat along with pressure is a conventionally known in the art combination known to be used in the bonding of chips (Lau).

With respect to claim 10, Lau teaches that the application of heat cures the resin thereby fixing the chip to the substrate.

It would have been obvious to one of ordinary skill in the art at the time of the invention to the heat and pressure combination of Lau in the invention of Hiroyuki and Takiar because it is a conventionally known method of bonding chips to substrate.

The use of conventional materials to perform there known functions in a conventional process is obvious. In re Raner 134 USPQ 343 (CCPA 1962).

Claims 11 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hiroyuki et al., JP 2000188369, in view of Takiar et al., US Patent 5,422,435, as applied to claim 8 above, and further in view of Okazaki et al., US Patent 6,269,999.

Both Hiroyuki and Takiar fail to teach the use of ultrasonic/supersonic waves in the bonding of solder balls attached a chip to a substrate.

Ukazaki teaches chip mounting using ultrasonic vibrations to bond a chip having balls mounted on its electrodes (abstract & Figures).

It would have been obvious to one of ordinary skill in the art at the time of the invention to the ultrasonic bonding of Okazaki in the invention of Hiroyuki and Takiar because it is a conventionally known method of bonding chips to substrates (1 , 21+).

The use of conventional materials to perform there known functions in a conventional process is obvious. In re Raner 134 USPQ 343 (CCPA 1962).

Claims 17 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hiroyuki et al., JP 2000188369, in view of Mitsuhiro, JP 03-106622, and Kumamoto et al., US Patent 6,632,704.

Hiroyuki teaches a device comprising:

[redacted]

(a) preparing a transfer mold (abstract) which is inherently provided with a cavity having first and second side surfaces facing each other and third and fourth surfaces facing each other and coming in contact with said first and second side surfaces;

(b) preparing a wiring substrate (3) having a main surface, preparing a first semiconductor chip (1a) fixed on said main surface of said wiring substrate and preparing a second semiconductor chip (1b) fixed on said first semiconductor chip;

(c) inherently placing said wiring substrate, said first semiconductor chip and said second semiconductor chip inside said cavity; and

(d) after said step (c), injecting resin concurrently from the plurality of resin injection entrances toward the second side surface of the cavity in order to seal and hold said first and second semiconductor chips,

wherein in said step (c), said wiring substrate, said first semiconductor chip and said second semiconductor chip are arranged in such a way that, on a cross section parallel to said third side surface of said cavity, the length of said first semiconductor chip exceeds the length of said second semiconductor chip;

wherein in said step (c), said wiring substrate, said first semiconductor chips, and said second semiconductor chips are arranged in such a way that, on a cross section parallel to said first side surface of said cavity, the length of each of said first semiconductor chips are smaller than the length of corresponding second semiconductor chips stacked on said first semiconductor chips. (figures).

Hiroyuki fails to teach the mold to be provided with a resin injection entrance created on said first side surface, and a ventilation hole created on said second side surface.

Kumamoto teaches a molded flip chip package having air vents formed in the mold opposite the runner [resin injection entrance] (3, 10-15).

While Kumamoto teaches encapsulating a single chip, the application of air vents on the side opposite the runner [resin injection entrances] would apply to any encapsulating situation.

It would have been obvious to one of ordinary skill in the art at the time of the invention to use the air vents of Kumamoto formed on the side opposite the runner [resin injection entrances] in the invention of Hiroyuki because Kumamoto teaches that the air vents allow displaced air in the mold to escape (3, 10-15).

Also, Hiroyuki fails to teach the use of a plurality of resin injection entrances.

Mitsuhiro teaches a semiconductor molding process wherein a resin is flowed into a cavity containing a semiconductor package wherein there exist 2 entrance gates (3), both on the same side of the cavity.

It would have been obvious to one of ordinary skill in the art to use the multiple resin entrance gates of Mitsuhiro in the transfer molding of Hiroyuki because Mitsuhiro teaches that heat can be absorbed effectively, pressure can be easily applied and the molding cycle time can be improved.

Claim 20 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hiroyuki et al., JP 2000188369, in view of Mitsuhiro, JP 03-106622 and Kumamoto et al., US Patent 6,632,704.

Hiroyuki teaches a device comprising:

(a) preparing a transfer mold (abstract) which is inherently provided with a cavity having first and second side surfaces facing each other and third and fourth side surfaces facing each other and coming in contact with said first and second side surfaces;

(b) preparing a wiring substrate (3) having a main surface, preparing a first semiconductor chips (1a) fixed on said main surface of said wiring substrate and preparing a second semiconductor chips (1b) fixed on said first semiconductor chips;

(c) inherently placing said wiring substrate, said first semiconductor chip and said second semiconductor chip inside said cavity; and

(d) after said step (c) injecting resin concurrently from the plurality of resin injection entrance toward the second side surface of the cavity in order to seal and hold said first and second semiconductor chips, wherein in said step (c), said wiring substrate, said first semiconductor chip and said second semiconductor chip are arranged in such a way that, on a cross section parallel to said third side surface of said cavity, the length of said first semiconductor chip exceeds the length of said second semiconductor chip,

wherein in said step (c), said wiring substrate, said first semiconductor chips, and said second semiconductor chips are arranged in such a way that, on a cross section

parallel to said first side surface of said cavity, the length of each of said first semiconductor chips are smaller than the length of corresponding second semiconductor chips stacked on said first semiconductor chips. (figures).

Hiroyuki fails to teach the mold to be provided with a resin injection entrance created on said first side surface, and a ventilation hole created on said second side surface.

Kumamoto teaches a molded flip chip package having air vents formed in the mold opposite the runner [resin injection entrance] (3, 10-15).

While Kumamoto teaches encapsulating a single chip, the application of air vents on the side opposite the runner [resin injection entrances] would apply to any encapsulating situation.

It would have been obvious to one of ordinary skill in the art at the time of the invention to use the air vents of Kumamoto formed on the side opposite the runner [resin injection entrances] in the invention of Hiroyuki because Kumamoto teaches that the air vents allow displaced air in the mold to escape (3, 10-15).

Also, while Hiroyuki fails to teach the use of a plurality of device areas on the substrate, a plurality of 1st chips and a plurality of 2nd chips, it would have been obvious to one of ordinary skill in the art to make a strip lead frame-type of wiring substrate where multiple individual chip stacks can be formed thereon.

The mere duplication of parts has no patentable significance unless a new and unexpected result is produced. In re Harza, 124 USPQ 378 (CCPA 1960).

Finally, Hiroyuki also fails to teach the use of a plurality of resin injection entrances.

Mitsuhiro teaches a semiconductor molding process wherein a resin is flowed into a cavity containing a semiconductor package wherein there exist 2 entrance gates (3), both on the same side of the cavity.

It would have been obvious to one of ordinary skill in the art to use the multiple resin entrance gates of Mitsuhiro in the transfer molding of Hiroyuki because Mitsuhiro teaches that heat can be absorbed effectively, pressure can be easily applied and the molding cycle time can be improved.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. US Patents 6,413,81; 6,309,916; 6,168,970; 5,920,768; 5,817,545; and 5,753,538 are all cited as teaching the use of air vents formed on a side opposite the resin injection entrance of an encapsulating mold.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to David A. Zarneke whose telephone number is (571)-272-1937. The examiner can normally be reached on M-F 10 AM-6PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kamand Cuneo can be reached on (571)-272-1957. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

David A. Zarneke
Primary Examiner
April 27, 2004